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U.S. **UTILITY** Patent Application

PATENT DATE

09/920192	CONT/PRIOR	CLASS 029	SUBCLASS 840	ART UNIT 3729	EXAMINER TOION	
Vivek Jai Thomas Kr Mohan Par	aútheim	*		; ;-		<i>*</i> .

Method for making an electronic circuit assembly

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TERMINAL		DRAWINGS		CLAIMS ALLOWED		
L DISCLAIMER	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
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The term of this patent shall not extend beyond the expiration date of U.S Patent. No.				ISSI	JE FEE	
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